selectively etching away said third insulating film so as to form a side wall insulating film including said third insulating film on each of both side faces of said first conductive film and said second insulating film and also to expose said semiconductor substrate in portions which are not covered with said side wall insulating film and not covered with said first conductive film;

diffusing impurities into said exposed portions of said semiconductor substrate so as to form a source and a drain in said semiconductor substrate;

forming a second conductive film to be a part of said buried conductive layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film and said side wall insulating film formed thereon;

forming a first mask layer on said second conductive film;

processing said first mask layer to have a pattern which is separated into both side portions as to said first conductive film;

forming a second mask layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film, said side wall insulating film, said second conductive film and said first mask layer formed thereon;

selectively etching away said second mask layer so as to leave a pattern of said second mask layer on each of both side faces of the pattern of said first mask layer; and

selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by openings smaller than the minimum processing size.

Please kindly add the following new claims:

21. A method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size, comprising:

forming a semiconductor element in a substrate;

forming a conductive layer over the semiconductor element and the substrate;

forming a first mask layer on the conductive layer;

patterning the first mask layer to form a slit dividing the first mask layer into at least two mask portions, the slit having a width equal in size to the minimum processing feature size and having side walls corresponding to end faces of the two mask portions;

forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit; and

etching the conductive layer using the first and second mask layers to separate the conductive layer into at least two conductive layer portions, the at least two conductive layer portions being separated by a distance which is less than the minimum processing feature size.

22. The method of claim 21 wherein the distance separating the at least two conductive layer portions is about 1/3 the minimum processing feature size.

23. The method of claim 21 further comprising contacting a structure

underlying the conductive layer through the at least two conductive layer portions.

24. The method of claim 23 wherein the structure underlying the conductive layer has the minimum processing feature size.

25. The method of claim 21 wherein each of the first mask layer and second mask layer is formed from an insulating film.

26. The method of claim 21 wherein the first mask layer is formed from a conductive film and the second mask layer is formed from an insulating film.

27. The method of claim 21 wherein each of the first mask layer and second mask layer is formed from a conductive film.

28. A method of forming a semiconductor device, comprising:

defining an active area in a substrate;

forming source and drain regions in the active area with a gate structure overlying the substrate therebetween;

forming a conductive layer over the substrate and the gate structure;

forming a first mask over the conductive layer;

performing photolithography to form a slit in a part of the first mask layer overlying the gate structure;

forming a second mask layer on the first mask layer and in the slit;

selectively etching away the second mask layer to leave the second

mask layer on side faces of the first mask layer in the slit; and

etching the conductive layer using the first and second mask layers as a mask, thereby patterning the conductive layer into at least two portions separated by a distance which is less than a minimum processing size.

29. The method of claim 28 wherein both the first mask layer and the second mask layer have etch rates slower than an etch rate of the conductive layer.

30. The method of claim 28 wherein each of the first mask layer and the second mask layer are formed from an insulating film.

31. A method of semiconductor manufacture comprising:

forming a first layer over a semiconductor substrate;

patterning the first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a lithographic process used during manufacture of the device;

forming a second layer on the sidewalls so as to reduce the width of the holes below the minimum feature size;

patterning a conductive layer beneath the first and second layers using the holes to form openings in the conductive layer that are smaller in size than the minimum feature size.

32. The method of claim 31 wherein the first layer and the second mask layer have etch rates slower than an etch rate of the conductive layer.

33. The method of claim 31 wherein the openings in the conductive layer are about 1/3 the minimum feature size.

34. A method of forming a semiconductor device, comprising:

defining an active area in a substrate;

forming source and drain regions in the active area;

forming a gate electrode overlying the substrate between the source and drain regions, the gate electrode having a width no larger than a minimum processing size available with a photolithographic process associated with forming the gate electrode;

forming a first layer over at least the active area of the substrate; and

forming a contact hole in the first layer in an area above the gate electrode, the contact hole having a width smaller than the minimum processing size of the photolithographic process.

35. The method of claim 34 further comprising contacting the gate electrode through the contact hole.

36. The method of claim 34 wherein forming the contact hole comprises:

forming a first mask on the first layer;

patterning the first mask to form a slit dividing the first mask into at least two mask portions, the slit having a width equal in size to the minimum

processing feature size and having side walls corresponding to end faces of the two mask portions;

forming a second mask on the slit sidewalls, thereby reducing the width of the slit; and

etching the first layer using the first and second mask to form the contact hole.

37. The method of claim 36 wherein forming the second mask comprises:

forming a second mask layer on the first mask and in the slit; and

selectively etching away the second mask to leave the second mask on side walls of the first mask in the slit.

38. A method of forming a semiconductor device, comprising:

forming a structure having a first width on a substrate;

forming a first layer over at least the structure; and

forming slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width, wherein the first width may be minimized as the second width is smaller than a minimum feature size achievable with a lithographic process used for making such device.

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40. A method of forming a semiconductor device, comprising:

defining an active area in a substrate with isolation structures, the isolation structure having a width no larger than a minimum processing size available with a photolithographic process associated with forming the isolation structure;